Improved Tx-to-Rx Isolation of Radar Transceivers Using Integrated Full Duplexer with PLL

Yeong Seok Choi, Choon Sik Cho and Young-Jin Kim
School of Electronics and Information Engineering
Korea Aerospace University
Goyang, Republic of Korea
ivory9675@naver.com, cscho@kau.ac.kr, youngjinkim@kau.ac.kr

***Abstract*— The isolation between transmitter and receiver for the radars is ultimately important since the transmitting radar signals can be penetrated the receiver directly in case a bad isolation is formed. This paper describes the isolation between the transceiver and the design of an integrated full duplexer using the phase locked loop (PLL). Although the antenna impedance varies arbitrarily, the PLL tracks the impedance variation in real time, leading to improvement of isolation between the transmitter and the receiver of radars. The full duplexer reduces the transmitter leakage up to 45 dB using the balance network along with the PLL in measurement.**

Keywords*— Balanced network, Integrated Full Duplexer, PLL, Transceiver, CMOS process, Impedance tracking.

I. INTRODUCTION

The continuous wave (CW) radar and the frequency modulated continuous wave (FMCW) radar require a good isolation between the transmitter and the receiver because the transmitting signal directly fed-back to the receiver may obstruct the desired radar operation. A full duplexer can be adopted in the radar transceivers to isolate the transmitter and the receiver when the same antenna is shared for transmitting and receiving signals. However, because of the bandwidth limitation, operating transmitter and receiver in the same frequency bands is considered for expanding system capacity in terms of frequency availability. The full duplexer can reduce the bandwidth requirement and maintain high isolation between the transmitter and the receiver. RF duplexer using a hybrid transformer and tunable CMOS integrated duplexer have been demonstrated in the wireless communication area where the full duplexed transmitter is devised to isolate transmitting signals in the receiver side as shown in Fig. 1 [1, 2].

In this work, an impedance tracking system using the phase locked loop (PLL) which can measure the transmitter leakage and tune the impedance of the balance network is suggested for radar transceivers as shown in Fig.2.

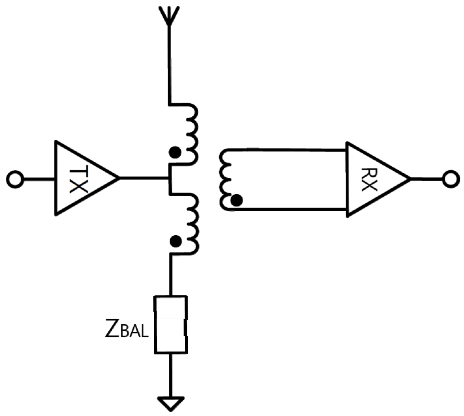

Fig. 1. The traditional integrated full duplexer transceiver [1,2].

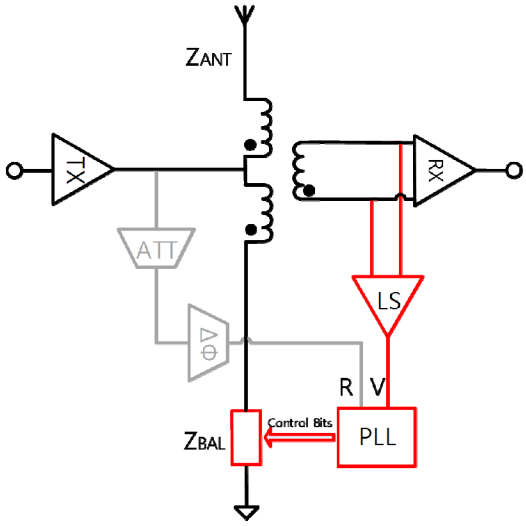

Fig. 2. The proposed integrated full duplexer transceiver with PLL.

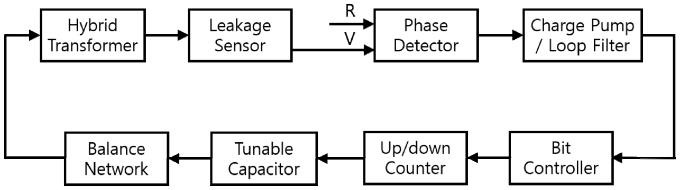

Fig. 3. Block diagram of the proposed integrated full duplexer transceiver with PLL.

II. The Proposed Integrated Full Duplexer Using Phase Locked Loop

A block diagram of the proposed full duplexer transceiver using PLL is shown in Fig. 3. Due to capacitance variation for some reasons such as a mismatch in process and an interaction with conductors, transmitter leakage increases. The ideal transmitter leakage in magnitude and phase is shown in Fig. 4 and Fig. 5, respectively. Using the phase of transmitter leakage, the varactor determines whether to increase or decrease the capacitance in the balance network [3-5].

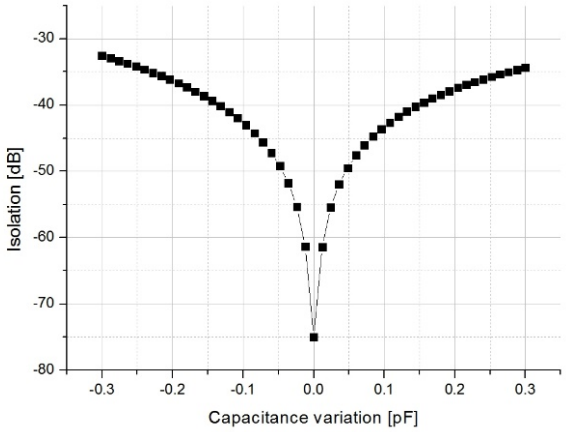

Fig. 4. Isolation between TX and RX by antenna capacitance variation.

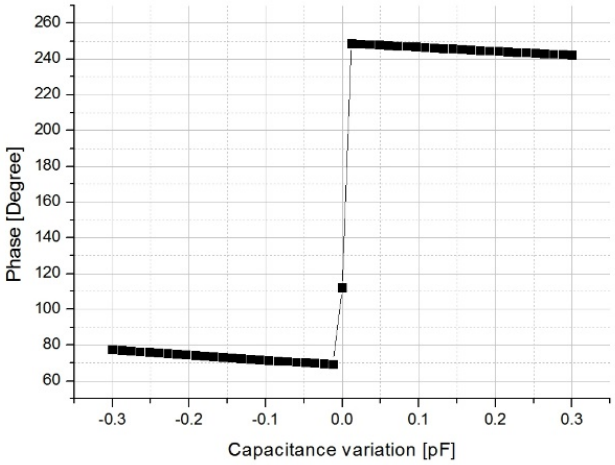

Fig. 5. Phase of the transmitter leakage by antenna capacitance variation.

III. Design of The Proposed Duplexer

A. Leakage Sensor

A leakage sensor is devised using one-stage differential-pair amplifier which can amplify the transmitter leakage sufficiently to detect the phase of leakage. Leakage sensor achieves gain of 46.5 dB, CMRR of 96 dB and bandwidth of 2.3 GHz.

B. Phase Detector

The phase detector consists of two D-flip flops (D-FF), one NAND gate, and several inverters refining the signals as shown in Fig. 6. D-FF detects the rising edge which can represent the phase of signal as described in Fig. 7. When both D-FFs are set, the value will be reset. The difference between the rising edges of transmitter leakage signal and the reference signal is transported to the charge pump.

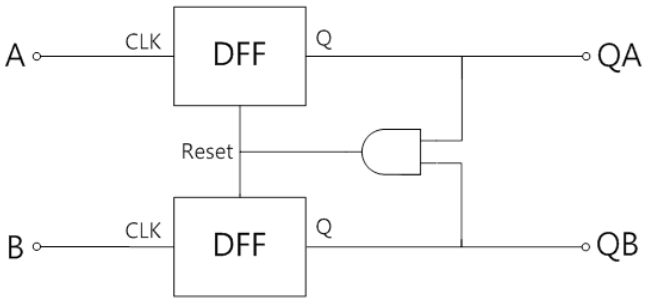

Fig. 6. Block diagram of the phase detector.

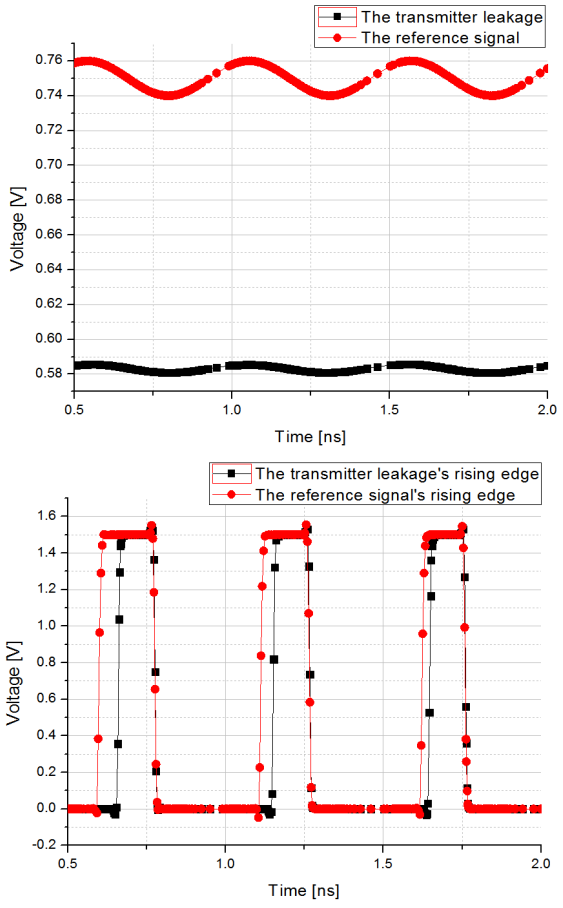

Fig. 7. Input and output voltages of the phase detector.

C. Charge Pump and Loop Filter

A charge pump detects the difference between the rising edges of transmitter leakage signal and the reference signal and adjusts the control voltage by charging or discharging the

capacitor of loop filter as shown in Fig.8. A loop filter plays the role of an LPF and a charge collector.

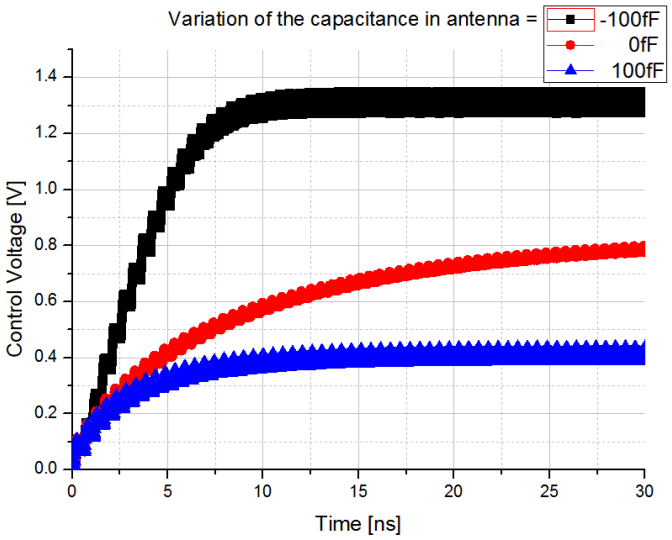

Fig. 8. The control voltage of charge pump and loop filter.

D. Bit Controller

Bit controller consists of six inverters, one NAND gate and one NOR gate as shown in Fig. 9. Two inverters in front divide the input voltage into three parts as shown in Fig. 10. And the NAND gate, the NOR gate and rest of the inverters determines whether to increase, decrease or maintain the control bits as shown in Table. 1.

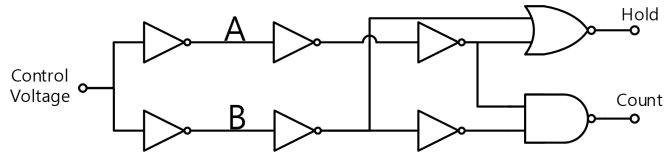

Fig. 9. Block diagram of Bit Controller.

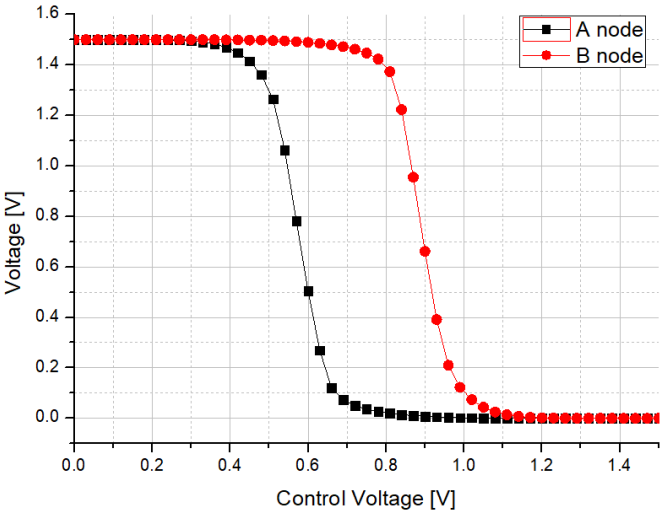

Fig. 10. Three parts of the control voltage at A and B nodes of the bit contolloer in Fig. 9.

TABLE I. TRUTH TABLE OF THE BIT CONTROLLER

Node		Output		Control Bits
A	B	COUNT	HOLD	
1	1	0	0	Decrease
0	1	X	1	Hold
0	0	1	0	Increase

E. Up/down Counter

Up/down counter consists of three JK flip-flops, four NOR gates, four AND gates and two inverters as shown in Fig. 11. According to COUNT bit, control bits increase or decrease, and HOLD bit maintains the control bits as shown in Table. 1.

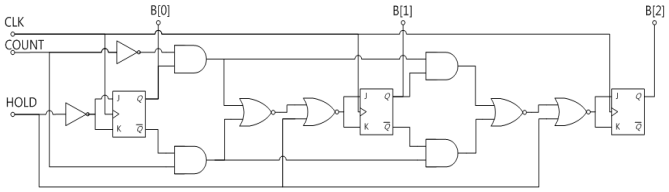

Fig. 11. Block diagram of Up/down counter

F. Tunable Capacitor

Tunable capacitor is placed in the balance network and the unit of tunable capacitor is 25fF as shown in Fig. 12.

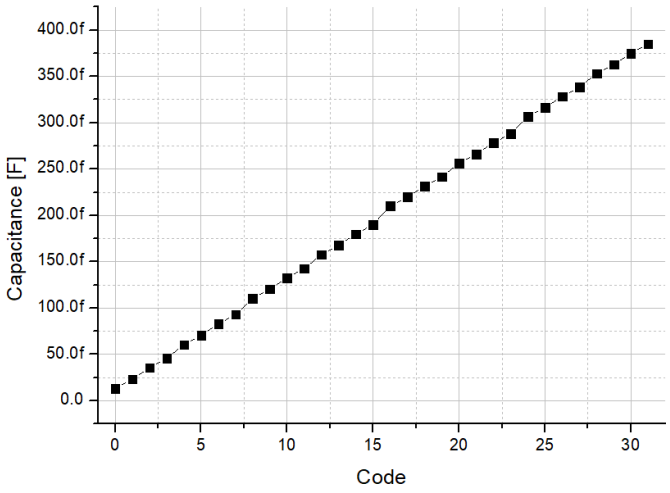

Fig. 12. Tunable capacitor with 25fF/step.

IV. MEASUREMENT RESULTS

The designed full duplexer with PLL is fabricated in 60nm RF CMOS technology as shown in Fig. 13. This chip occupies an area of 0.495mm^2 and wire bonding operation on PCB is carried out for measurement. The fabricated PCB in shown in Fig. 14. Since the designed full duplexer has differential output ports, an active balun is linked with the fabricated PCB for accurate measurement.

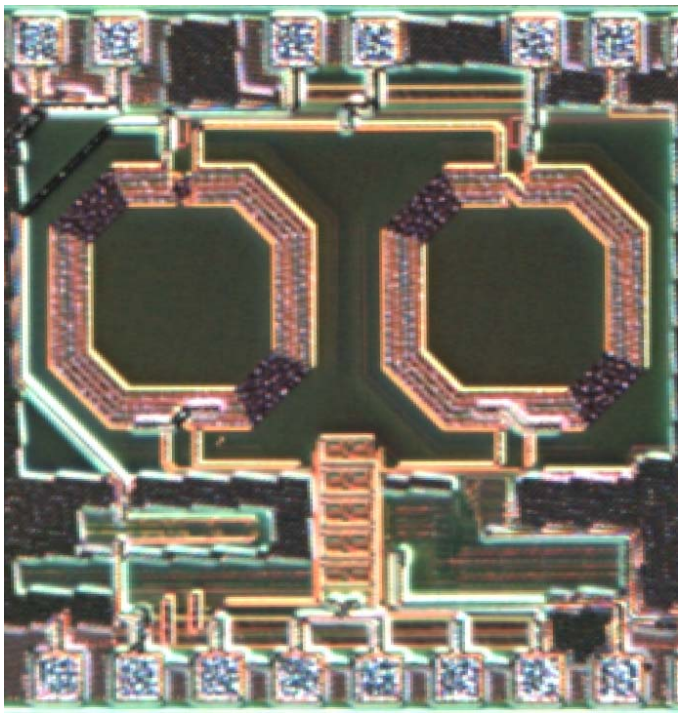

Fig. 13. Photograph of the designed full duplexer with PLL in 60nm RF CMOS process.

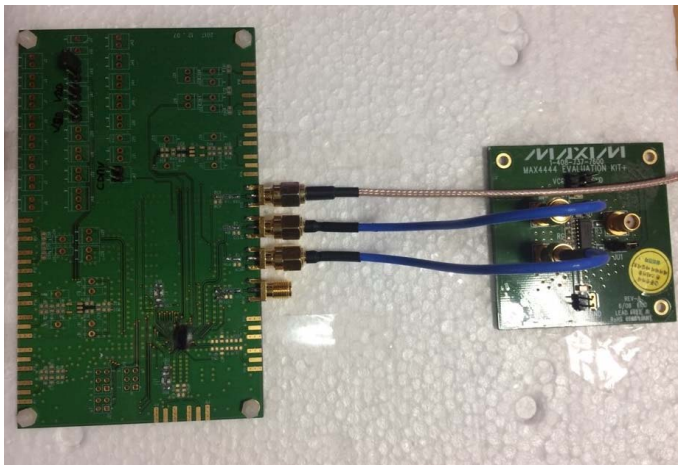

Fig. 14. The fabricated PCB for the designed full duplexer connected to an active balun outside for measurement.

The designed full duplexer with PLL consumes DC power of 79.5 mW with 1.5V DC voltage. When the phase of the reference signal (R in Fig. 3) is compensated by 160 degrees in this work, the control voltage resulting from the charge pump is maintained to be 711 mV constantly. Therefore, the control bits can keep the capacitance of tunable capacitor constant. The measured transmitter leakages are shown with respect to the control voltage of the charge pump (Vcp) varying the capacitance of balance network and antenna in Fig. 15. This graph shows that the isolation increases up to 45 dB when the capacitance value of the antenna and control voltage of the charge pump are optimized.

V. CLUSION

The proposed full duplexer with PLL optimized isolation in real time between the transmitter and the receiver by tracking the impedance variation of the antenna. In addition, impedance tracking can be achieved. The designed full duplexer with PLL consumes DC power of 79.5 mW and occupies an area of 0.495 mm^2.

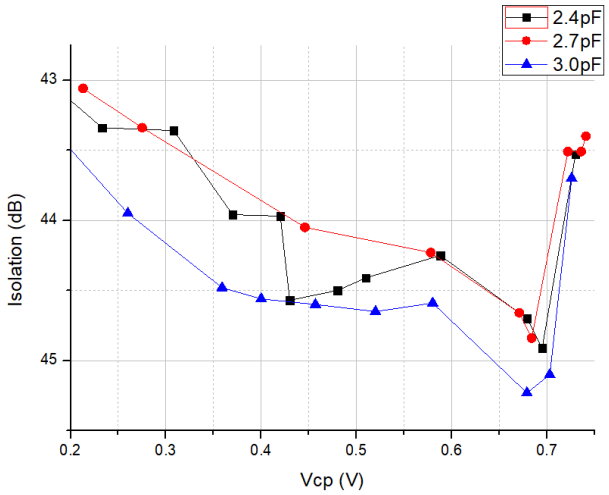

Fig. 15. The measured transmitter leakages.

VI. CONACKNOWLEDGMENT

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